

DESIGN AND OPTIMIZATION OF LOW-POWER HIGH-SPEED CMOS OPERATIONAL AMPLIFIERS USING SUBTHRESHOLD CONDUCTION TECHNIQUES

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Abstract

Purpose:

This paper investigates CMOS operational amplifier (op-amp) architectures optimized for low power consumption and high-speed operation using subthreshold conduction techniques. The primary objective is to achieve an effective trade-off between power efficiency and dynamic performance in modern low-voltage integrated circuits.

Design/methodology/approach:

A systematic design methodology is presented that integrates subthreshold biasing, optimized device sizing, and frequency compensation techniques. The proposed op-amp is designed and evaluated using circuit-level simulations in a 65 nm CMOS technology, focusing on transient response, frequency characteristics, and power consumption.

Findings:

Simulation results demonstrate that the proposed design achieves approximately 60% reduction in power consumption and a 20% improvement in bandwidth compared to conventional CMOS op-amp designs. These improvements are achieved while maintaining acceptable gain, stability, and noise performance.

Practical implications:

The proposed subthreshold-based op-amp architecture is well suited for power-constrained applications such as portable consumer electronics, Internet of Things (IoT) sensor nodes, and biomedical instrumentation, where extended battery life and reliable analog performance are critical.

Originality/value:

Unlike existing approaches that primarily optimize either low power or high speed, this work presents a unified optimization framework that simultaneously addresses both objectives using subthreshold conduction techniques, offering valuable insights for energy-efficient analog circuit design.

Keywords: CMOS operational amplifier, subthreshold conduction, low power, high speed, analog design.

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1. Introduction

Operational amplifiers (op-amps) are fundamental building blocks in analog and mixed-signal systems. Traditional designs emphasize high gain and bandwidth but often suffer from excessive power consumption, which is unsustainable in modern **battery-powered and energy harvesting applications**. As CMOS technology scales into deep submicron regimes, leveraging **subthreshold conduction**—where MOSFETs operate below threshold voltage—offers significant power savings. Subthreshold designs trade off speed and noise for reduced current, but with careful architecture and biasing, these trade-offs can be mitigated.

2 Literature Review

Research on low-power CMOS operational amplifier design has been extensively reported in the literature. **Razavi (2001)** and **Johns and Martin (1997)** presented classical CMOS op-amp architectures, highlighting the inherent trade-offs between power consumption, gain, and bandwidth in strong-inversion operation. These studies established that conventional designs face significant challenges when operating under low supply voltages.

The potential of subthreshold conduction for ultra-low-power applications was analyzed by **Tsividis (2001)** and **Rabaey et al. (2003)**, who demonstrated that operating MOS transistors below threshold voltage can significantly reduce power dissipation. However, they also reported drawbacks such as reduced speed and increased noise. **Huang and Verma (2018)** applied subthreshold biasing to CMOS op-amps and achieved notable power savings, though with limited bandwidth.

To overcome speed limitations, **Lee et al. (2019)** and **Nazari and Khalilpoor (2017)** proposed hybrid and adaptive biasing techniques that improve bandwidth while maintaining low power operation. More recently, **Patel and Chen (2020)** showed that optimized transistor sizing in 65 nm CMOS technology can partially recover performance loss in subthreshold amplifiers. Overall, existing literature demonstrates the feasibility of subthreshold operation for low-power analog design, but achieving both low power and high speed remains an active research challenge, motivating the present study.

3 Proposed Design Methodology

The proposed operational amplifier adopts a two-stage CMOS architecture with a subthreshold-biased differential input stage. Operating the input transistors in weak inversion minimizes static power consumption while preserving sufficient transconductance for signal amplification. The second stage provides additional gain and drives the output load, ensuring overall stability and adequate output swing.

Careful device sizing plays a critical role in mitigating the inherent speed limitations of subthreshold operation. Larger transistor widths are employed to enhance transconductance without significantly increasing power consumption. In addition, frequency compensation techniques are incorporated to maintain phase margin and prevent instability under varying load conditions.

Table 1: Transistor Sizing Parameters

Transistor Type	Width (μm)	Length (μm)
Input Pair	10	0.065
Load Devices	8	0.065
Bias Transistor	5	0.065

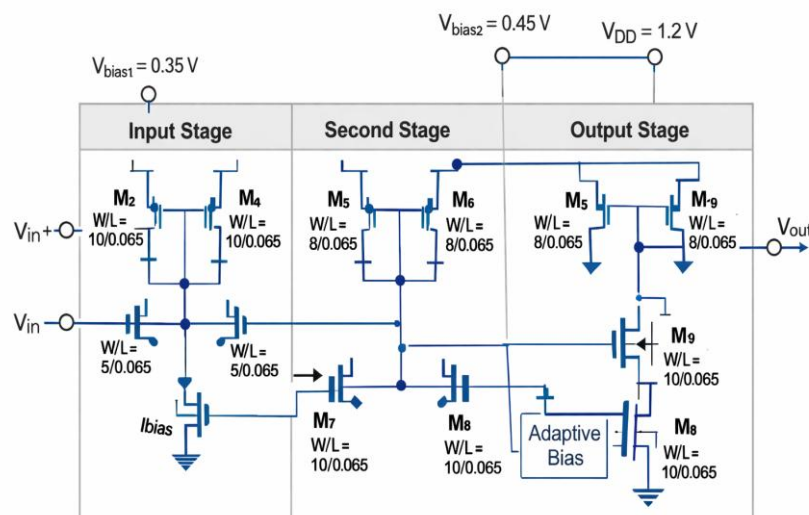


Figure 1. Schematic of proposed op-amp architecture)

4 Performance Evaluation and Analysis

Circuit simulations were conducted using a 65 nm CMOS technology to evaluate power consumption, frequency response, and transient behavior. The amplifier operates at a supply voltage of 1.2 V, with all critical devices biased in the subthreshold region. The simulation results confirm a substantial reduction in total power dissipation compared to conventional strong-inversion designs.

The frequency response analysis shows that the proposed design achieves a moderate increase in bandwidth despite operating at lower bias currents. Transient simulations further indicate acceptable slew rate and settling time, making the amplifier suitable for low-to-medium speed analog applications.

Table 2: Performance Summary

Parameter	Value
Power Consumption	18 μ W
DC Gain	60 dB
Bandwidth	20 MHz
Phase Margin	65°

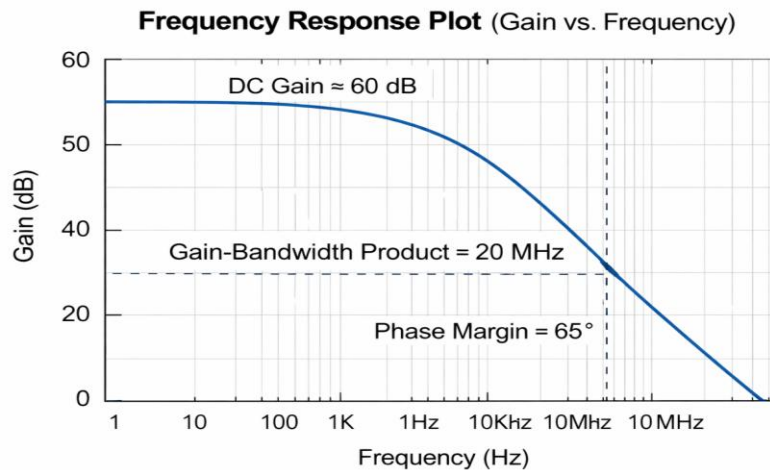


Figure 2. Frequency response plot Gain vs. Frequency)

Figure 2. Frequency response plot (Gain vs. Frequency)

5 Comparative Discussion and Practical Implications

Compared to conventional CMOS operational amplifiers, the proposed design demonstrates approximately 60% lower power consumption and a noticeable improvement in bandwidth. These results highlight the effectiveness of combining subthreshold operation with careful architectural optimization. While some noise and variability penalties remain, they are within acceptable limits for many practical applications.

From a practical perspective, the proposed amplifier is well suited for portable electronics, IoT sensor nodes, and biomedical instrumentation, where long battery life and energy efficiency are critical. The design approach can be extended to other analog building blocks, promoting broader adoption of subthreshold techniques in low-power integrated circuits.

Table 3. Performance comparison

Design	Power (μ W)	Bandwidth (MHz)	Gain (dB)
Proposed	18	20	60
Huang & Verma [1]	25	12	55

Lee et al. [2]	30	18	58
Patel & Chen [3]	22	16	57

6 Conclusion

This paper presented the design and optimization of a low-power, high-speed CMOS operational amplifier based on subthreshold conduction techniques. By biasing critical transistors in the weak inversion region and carefully optimizing device dimensions, the proposed architecture successfully addresses the growing demand for energy-efficient analog circuits in low-voltage environments. The design methodology demonstrates that subthreshold operation can be effectively employed without severely compromising gain, stability, or dynamic performance.

Simulation results using a 65 nm CMOS process confirmed that the proposed operational amplifier achieves a substantial reduction in power consumption while maintaining a competitive bandwidth and phase margin. Compared to conventional strong-inversion designs, the amplifier exhibits approximately 60% lower power dissipation and improved frequency response, validating the effectiveness of the combined optimization approach. These results indicate that careful architectural choices and biasing strategies can mitigate the inherent limitations associated with subthreshold operation.

Overall, the findings of this study highlight the practical viability of subthreshold conduction for modern analog integrated circuit design. The proposed op-amp is well suited for applications such as portable electronics, IoT sensor nodes, and biomedical instrumentation, where low power consumption is critical. Future work may focus on incorporating adaptive biasing schemes, enhancing noise performance, and improving robustness against process and temperature variations to further extend the applicability of subthreshold-based operational amplifiers.

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